Precheck guide

Install Volare and create the correct PDK:

Update Makefile:

The first important step is to update your Makefile which is located in the *caravel_user_project_analog* directory or *caravel_user_project* for digital projects. In this file there are two things that need to be changed, the MPW_TAG variable and the OPEN_PDKS_COMMIT variable. These are both located at the top of the file and at the time of writing should be changed to match the images below.

```
MPW_TAG ?= 2024.09.13-1
```

```
export OPEN_PDKS_COMMIT?=0fe599b2afb6708d281543108caf8310912f54af
```

IMPORTANT: These may change with time and you'll have to monitor or ask on slack if something has changed.

Install volare and make PDK:

Now that the makefile is updated we can run the following commands to install volare and make the correct version of the PDK. First we must set some global variables in order to place things in the correct spots.

```
export CARAVEL_ROOT=/home/kivimagi/reram/caravel_user_project_analog/caravel
export PDK=sky130B
export PDK_ROOT="/home/kivimagi/PDK"
```

- PDK_ROOT will be the directory where you install the PDK
- PDK is set to either sky130B or sky130A for our purposes we use sky130B
- CARAVEL_ROOT should point to the caravel directory located in the same directory as the Makefile we edited previously

Once these variables are set run the following command to install volare.

```
pip3 install --user volare
```

After this is complete run `volare ls` to verify that it installed correctly. If nothing happens you will need to add the directory that volare installed to to your path. The command for that will look similar to the following. In my case volare installed to *.local/bin.*

```
export PATH="/home/kivimagi/.local/bin:$PATH"
```

A successful volare ls should look similar to this:

```
(toolchain) [kivimagi@co2050-22 reram]$ volare ls
In /home/kivimagi/PDK/volare/sky130/versions:
├── 0fe599b2afb6708d281543108caf8310912f54af (2024.08.17) (enabled)
└── 6d4d11780c40b20ee63cc98e645307a9bf2b2ab8 (2024.02.11)
```

Now we are going to create the PDK. Run the following command.

```
make pdk-with-volare
```

The output should look like something like this:

```
Version 0fe599b2afb6708d281543108caf8310912f54af not found locally, attempting to download…
Downloading common.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_fd_io.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_fd_pr.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_fd_sc_hd.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_fd_sc_hvl.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_ml_xx_hd.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Downloading sky130_sram_macros.tar.zst… ━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━━ 100% 0:00:00
Version 0fe599b2afb6708d281543108caf8310912f54af enabled for the sky130 PDK.
make[1]: Leaving directory '/home/kivimagi/reram/caravel_user_project_analog'
(toolchain) [kivimagi@co2050-22 caravel_user_project_analog]$
```

You should be able to see that the value we set OPEN_PDKS_COMMIT to in the makefile is the version that has been enabled.

Setup and run precheck:

Make precheck:

Next we will create the precheck. To do this run the command

- **make precheck**

From the *caravel_user_project_analog directory.* From this point unless otherwise specified everything will be run from this directory. If successful this should create a directory called *mpw_precheck* in your home directory.

Prepare to run precheck:

There are a few files that need to be edited or placed into the proper locations before we can run precheck.

Layout and schematic files:

If you have gotten to this point you should have created these two files:

- user_analog_project_wrapper.gds
- user_analog_project_wrapper.spice

Precheck is very particular about where these files are located so it is important that they are placed in the correct spots.

The *user_analog_project_wrapper.spice* file created from the schematic should be placed into the *xschem* directory as well as the *netgen* directory, if there is already a file here named that either overwrite it or remove it before copying your file there.

NOTE: The file copied to *netgen* must have all comments removed from it. These are any lines that start with either an * or a **. If you do not do this the precheck will throw an error.

The *user_analog_project_wrapper.gds* file needs to be placed into the *gds* directory and should be the only thing in that directory. Once again remove or overwrite any files that are already there, if applicable.

```
(toolchain) [kivimagi@co2050-22 gds]$ pwd
/home/kivimagi/reram/caravel_user_project_analog/gds
(toolchain) [kivimagi@co2050-22 gds]$ ls
user_analog_project_wrapper.gds
(toolchain) [kivimagi@co2050-22 gds]$
```

Edit user_defines.v:

There is a file called user_defines.v that must be updated in order to pass the precheck. It is located here:

- **~/caravel_user_project_analog/verilog/rtl/user_defines.v**

This file is used for determining what what mode the GPIO pins will operate as such as input output, bidirectional etc. The value GPIO_MODE_INVALID in Lines 55-90 needs to be changed to one of the variables given at the top of the file based on what you want the pin to operate as. These picture show an example where all pins have been set to bidirectional pins.

Unset:

```
55 `define USER_CONFIG_GPIO_5_INIT  `GPIO_MODE_INVALID
56 `define USER_CONFIG_GPIO_6_INIT  `GPIO_MODE_INVALID
57 `define USER_CONFIG_GPIO_7_INIT  `GPIO_MODE_INVALID
58 `define USER_CONFIG_GPIO_8_INIT  `GPIO_MODE_INVALID
59 `define USER_CONFIG_GPIO_9_INIT  `GPIO_MODE_INVALID
60 `define USER_CONFIG_GPIO_10_INIT `GPIO_MODE_INVALID
61 `define USER_CONFIG_GPIO_11_INIT `GPIO_MODE_INVALID
62 `define USER_CONFIG_GPIO_12_INIT `GPIO_MODE_INVALID
63 `define USER_CONFIG_GPIO_13_INIT `GPIO_MODE_INVALID
```

Bidirectional:

```
55 `define USER_CONFIG_GPIO_5_INIT  `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
56 `define USER_CONFIG_GPIO_6_INIT  `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
57 `define USER_CONFIG_GPIO_7_INIT  `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
58 `define USER_CONFIG_GPIO_8_INIT  `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
59 `define USER_CONFIG_GPIO_9_INIT  `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
60 `define USER_CONFIG_GPIO_10_INIT `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
61 `define USER_CONFIG_GPIO_11_INIT `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
62 `define USER_CONFIG_GPIO_12_INIT `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
63 `define USER_CONFIG_GPIO_13_INIT `GPIO_MODE_MGMT_STD_BIDIRECTIONAL
```

Edit Readme.md:
This is a simple one the default Readme file just need to be updated to a description of your project. Something more in depth or as simple as this:

```
1 # reram 1t1r precheck test
```

Run precheck:

Run the following command to start precheck:

- **make run-precheck**

If you have done all the steps correctly you should be able to pass precheck for any design that does not include reram cells.

Reram precheck LVS errors and solutions:

Reram cells require a little more effort to push though precheck. This will cover the potential errors that can happen and how to solve them. The easiest way to find the error is from the lvs.report file, the location of which will be displayed in the terminal as the precheck runs.

Property errors:

There are two property errors that can occur from the reram cell.

The first is a Tfilament error and looks like this:

```
Netlists match uniquely with property errors.
Circuit 1 1T1R instance sky130_fd_pr_reram__reram_cell:R1 property "Tfilament_0" has no match in circuit 2.
```

If you run into this error, you have done something wrong in the steps above or you do not have the newest PDK version as this one is solved by using the correct PDK version given above

The second property error is the area_ox error and looks like this:

```
Netlists match uniquely with property errors.
x1T1R:1T1R_0/sky130_fd_pr_reram__reram_cell_X:XR1/sky130_fd_pr_reram__reram_cell:0 vs. 1T1R:1/sky130_fd_pr_reram__reram_cell:R1:
Property area_ox in circuit1 has no matching property in circuit2
```

This means that there is a parameter in the *user_analog_project_wrapper.gds* file that does not match with the schematic side. To fix this we must add this parameter to the *user_analog_project_wrapper.spice* file located in the xschem directory.

Inside of *user_analog_project_wrapper.spice* there will be subcircuits that contain **sky130_fd_pr_reram__reram_cell.** For each **sky130_fd_pr_reram__reram_cell** the string **area_ox=1** needs to be added at the end of the line. An example is shown below.

- **Subcircuit:**

```
.subckt 1T1R BL WL VSS SL
*.PININFO SL:B VSS:B WL:B BL:B
XR1 BL net1 sky130_fd_pr_reram__reram_cell Tfilament_0=3.8e-9
XM1 net1 WL SL VSS sky130_fd_pr__nfet_g5v0d10v5 L=0.5 W=7 nf=1 m=1
.ends
```

- **Sky130_fd_pr_reram__reram_cell line without update:**

```
XR1 BL net1 sky130_fd_pr_reram__reram_cell Tfilament_0=3.8e-9
```

- **Updated Sky130_fd_pr_reram__reram_cell line:**

```
XR1 BL net1 sky130_fd_pr_reram__reram_cell Tfilament_0=3.8e-9 area_ox=1
```

- **Updated subcircuit:**

```
.subckt 1T1R BL WL VSS SL
*.PININFO SL:B VSS:B WL:B BL:B
XR1 BL net1 sky130_fd_pr_reram__reram_cell Tfilament_0=3.8e-9 area_ox=1
XM1 net1 WL SL VSS sky130_fd_pr__nfet_g5v0d10v5 L=0.5 W=7 nf=1 m=1
.ends
```

Disconnected nodes:

If LVS in your precheck is failing and you have something similar to this image in your lvs.report file:

```
Cell sky130_fd_pr_reram__reram_cell (0) disconnected node: TE
Cell sky130_fd_pr_reram__reram_cell (0) disconnected node: BE
Flattening instances of sky130_fd_pr_reram__reram_cell in cell sky130_fd_pr_reram__reram_cell (1) makes a better
match
Making another compare attempt.

Cell sky130_fd_pr_reram__reram_cell (0) disconnected node: TE
Cell sky130_fd_pr_reram__reram_cell (0) disconnected node: BE
Flattening instances of sky130_fd_pr_reram__reram_cell in cell sky130_fd_pr_reram__reram_cell (1) makes a better
match
Making another compare attempt.
```

The solution is to remove the following code from your *user_analog_project_wrapper.spice* netlist.

Remove this:

```
**** begin user architecture code

.subckt sky130_fd_pr_reram__reram_cell TE BE Tfilament_0=3.3e-9 area_ox=0.1024e-12
N1 TE BE nFilament sky130_fd_pr_reram__reram_model
.ic v(nFilament)={Tfilament_0*1.0e9}
.ends sky130_fd_pr_reram__reram_cell

.model sky130_fd_pr_reram__reram_model sky130_fd_pr_reram__reram_module  area_ox = 0.1024e-12  Tox =
+ 5.0  Tfilament_max = 4.9  Tfilament_min = 3.3  Eact_generation = 1.501  Eact_recombination  = 1.500
+  I_k1  = 6.140e-5  Tfilament_ref = 4.7249  V_ref = 0.430  velocity_k1 = 150  gamma_k0  = 16.5  gamma_k1
+  = -1.25  Temperature_0 = 300  C_thermal = 3.1825e-16  tau_thermal = 0.23e-9  t_step  = 1.0e-9
+  smoothing = 1e-7  Kclip = 200

.control
pre_osdi
+ /home/kivimagi/reram/caravel_user_project/dependencies/pdks/sky130B/libs.tech/ngspice/sky130_fd_pr_reram__reram_module.osdi
.endc
```

Link to slack channel involving this information:

[Slack Conversation]